

05-25-06

IFW

Docket No. 8201/Y01/SYNX/JW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Mail Stop Amendment
 Commissioner for Patents
 P.O. Box 1450
 Alexandria, VA 22313-1450

Re: Inventor(s): Michael R. Rice, Eric A. Englhardt, Vinay Shah, Martin R. Elliott, Robert B. Lowrance and Jeffrey C. Hudgens
 Title: SYSTEMS AND METHODS FOR TRANSFERRING SMALL LOT SIZE SUBSTRATE CARRIERS BETWEEN PROCESSING TOOLS
 Serial No.: 10/764,620
 Filed: January 26, 2004
 Examiner: Kasenge, Charles R
 Group Art Unit: 2125



Transmitted herewith is:

- ☒ PTO Form 1449;
☒ Information Disclosure Statement, and sixteen cited references (copy of sixteen references enclosed); and
☒ Return Postcard.

FEE CALCULATION					
Fee Items	Claims Filed	Included With Basic Fee	Extra Claims	Fee Rate	Total
Total Claims	N/A	- 20 =	-0-	X \$50.00	\$0.00
Independent Claims	N/A	- 3 =	-0-	X \$200.00	\$0.00
Basic Filing Fee (\$300.00), Utility Search Fee (\$500.00), Utility Examination Fee (\$200.00)				\$1000.00	\$0.00
TOTAL FEES					PAID

☒ The Commissioner is hereby authorized to charge \$180.00 to Deposit Account No. 04-1696.

☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 04-1696. A duplicate copy of this transmittal is enclosed.

☒ Please address all future correspondence to: **Customer # 41161**
Dugan & Dugan, PC
55 South Broadway
Tarrytown, NY 10591

I hereby certify that this correspondence is being deposited with the United States Postal Service as express mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Express Mail Receipt No. EV605116041US

Date of Deposit: 5/23/06

Signature: [Signature]

Respectfully submitted,

[Signature]
 Brian M. Dugan
 Registration No. 41,720
 (914) 332-9081



Express Mail Label No. EV605116041US

PATENTS
8201/Y01/SYNX/JW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s) : Michael R. Rice et al.
Serial No. : 10/764,620
Filed : January 26, 2004
For : SYSTEMS AND METHODS FOR TRANSFERRING SMALL
LOT SIZE SUBSTRATE CARRIERS BETWEEN
PROCESSING TOOLS
Group Art Unit : 2125
Customer No. : 41161
Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with 37 C.F.R. §§ 1.56 and 1.97,
applicants wish to call the attention of the Examiner to the
following references:

Foreign Art Reference No. JP 08249044 A (Japan)
Foreign Art Reference No. JP 09115817 A (Japan)
Foreign Art Reference No. JP 10135096 A (Japan)
Foreign Art Reference No. JP 11176717 A (Japan)
Foreign Art Reference No. JP 11296208 A (Japan)
Foreign Art Reference No. JP 2001332464 A (Japan)

Foreign Art Reference No. JP 2003007584 A (Japan)

Foreign Art Reference No. DE 19715974 A1 (Germany)

Przewlocki, H. et al., "DIASTEMOS-computerized system of IC manufacturing control and diagnostics", 1990, Elektronika, Vol. 31 No. 11-12, Pgs. 38-40, Polish Language. (Abstract only)

Juba, R. C. et al., "Production improvements using a forward scheduler", 1996, Seventeenth IEEE/CPMT International Electronics Manufacturing Technology Symposium 'Manufacturing Technologies - Present and Future', Pg. 205-9.

Houmin, Yan et al., "Testing the robustness of two-boundary control policies in semiconductor manufacturing", May 1996, IEEE Transactions on Semiconductor Manufacturing, Vol. 9 No. 2, Pg. 285-8.

Lopez, M. J. et al., "Performance models of systems of multiple cluster tools", 1996, Nineteenth IEEE/CPMT International Electronics Manufacturing Technology Symposium. Proceedings 1996 IEMT Symposium, Pgs. 57-65.

Iriuchijima, K. et al., "WIP allocation planning for semiconductor factories", 1998, Proceedings of the 37th IEEE Conference on Decision and Control, Vol. 3, Pg. 2716-21.

Weiss, M., "New twists on 300 mm fab design and layout", July 1999, Semiconductor International, Vol. 22 No. 8, Pgs. 103-4, 106, 108.

Van Antwerp, K. et al., "Improving work-in-progress visibility with active product tags YASIC manufacture", Oct. 1999, Micro, Vol. 17 No. 9, Pgs. 67-9, 72-3.

Wei Jun-Hu et al., "Optimization methodology in simulation-based scheduling for semiconductor manufacturing", Oct. 2000, Information and Control, Vol. 29 No. 5, Pg. 425-30, Chinese language. (Abstract only)

Please charge deposit account No. 04-1696 in the amount of \$180.00 for consideration of this information disclosure statement under 37 C.F.R. § 1.97(c)(2).

These references are also listed on the accompanying Information Disclosure Statement (Form PTO-1449).

Consideration of the foregoing in relation to this patent application is respectfully requested.

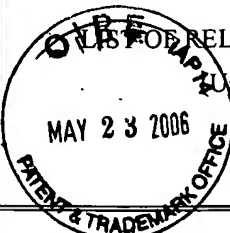
Respectfully Submitted,



Brian M. Dugan, Esq.
Registration No. 41,720
Dugan & Dugan, PC
Attorneys for Applicants
(914) 332-9081

Dated:

5/23/06
Tarrytown, New York

U.S. Department of Commerce, Patent and Trademark Office <div style="display: flex; align-items: center; justify-content: center;">  <div style="margin-left: 20px;"> (Use several sheets if necessary) </div> </div>				Docket No.: 8201/Y01/SYNX/JW		Serial No.: 10/764,620	
				Applicants: Michael R. Rice, et al			
				Filing Date: January 26, 2004		Group: 2125	
U.S. Patent Documents							
*Examiner Initial		Document Number	Issue Date	Name	Class	Subclass	Filing Date If Appropriate
	US-1						
	US-2						
	US-3						
	US-4						
	US-5						
	US-6						
	US-7						
	US-8						
	US-9						
	US-10						
	US-11						
Foreign Patent Documents							
							Translation
		Document Number	Date	Country	Class	Subclass	Yes No
	F-1	JP 08249044 A	09/27/96	Japan			X
	F-2	JP 09115817 A	05/02/97	Japan			X
	F-3	JP 10135096 A	05/22/98	Japan			X
	F-4	JP 11176717 A	07/02/99	Japan			X
	F-5	JP 11296208 A	10/29/99	Japan			X
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
	OT-1	Przewlocki, H. et al., "DIASTEMOS-computerized system of IC manufacturing control and diagnostics", 1990, Elektronika, Vol. 31 No. 11-12, Pgs. 38-40, Polish Language. (Abstract only)					
	OT-2	Juba, R. C. et al., "Production improvements using a forward scheduler", 1996, Seventeenth IEEE/CPMT International Electronics Manufacturing Technology Symposium 'Manufacturing Technologies - Present and Future', Pg. 205-9.					
	OT-3	Houmin, Yan et al., "Testing the robustness of two-boundary control policies in semiconductor manufacturing", May 1996, IEEE Transactions on Semiconductor Manufacturing, Vol. 9 No. 2, Pg. 285-8.					
Examiner			Date Considered				

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

U.S. Department of Commerce, Patent and Trademark Office LIST OF RELEVANT ART CITED BY APPLICANT (Use several sheets if necessary)				Docket No.: 8201/Y01/SYNX/JW		Serial No.: 10/764,620	
				Applicants: Michael R. Rice, et al			
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U.S. Patent Documents							
*Examiner Initial	Document Number	Issue Date	Name	Class	Subclass	Filing Date If Appropriate	
	US-12						
	US-13						
	US-14						
	US-15						
	US-16						
	US-17						
	US-18						
	US-19						
	US-20						
	US-21						
	US-22						

Foreign Patent Documents							Translation	
	Document Number	Date	Country	Class	Subclass	Yes	No	
	F-6	JP 2001332464 A	11/30/01	Japan		X		
	F-7	JP 2003007584 A	01/10/03	Japan		X		
	F-8	DE 19715974 A1	10/22/98	Germany		Abstract		
	F-9							
	F-10							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)	
OT-4	Lopez, M. J. et al., "Performance models of systems of multiple cluster tools", 1996, Nineteenth IEEE/CPMT International Electronics Manufacturing Technology Symposium. Proceedings 1996 IEMT Symposium, Pgs. 57-65.
OT-5	Iriuchijima, K. et al., "WIP allocation planning for semiconductor factories", 1998, Proceedings of the 37th IEEE Conference on Decision and Control, Vol. 3, Pg. 2716-21.
OT-6	Weiss, M., "New twists on 300 mm fab design and layout", July 1999, Semiconductor International, Vol. 22 No. 8, Pgs. 103-4, 106, 108.

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	US-26						
	US-27						
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	US-29						
	US-30						
	US-31						
	US-32						
	US-33						

Foreign Patent Documents							Translation	
	Document Number	Date	Country	Class	Subclass	Yes	No	
	F-11							
	F-12							
	F-13							
	F-14							
	F-15							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)		
OT-7	Van Antwerp, K. et al., "Improving work-in-progress visibility with active product tags YASIC manufacture", Oct. 1999, Micro, Vol. 17 No. 9, Pgs. 67-9, 72-3.	
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OT-9		

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